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I, the below named and addressed translator, hereby declare that I am the translator of the certified copy of Corporation Registration attached and that the following is a true translation to the best of my knowledge and belief.

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YoungHun Jang

Young-Hun Jang

2F-3F, Line Bldg., 823-30
Yeoksam-dong, Kangnam-gu
Seoul 135-613
Republic of Korea

[Abstract of the Disclosure]

[Abstract]

The present invention relates to a method for fabricating a semiconductor device that forms a capacitor in the same level of a simultaneously in a damascene process, and this invention brings about the effect of obtaining a capacitance of a high capacity needed for logic elements without increasing the number of layers for fabricating a capacitor by forming a three-dimensional capacitor in the damascene pattern while maintaining the conventional processes in a damascene interconnection process.

[Representative Figure]

Figure 1

[Index]

Serpentine, Capacitor, Damascene, Copper, Via

[Specification]

[Title of Invention]

METHOD OF FORMING SEMICONDUCTOR DEVICE WITH CAPACITOR AND METAL-INTERCONNECTION IN DAMASCENE PROCESS

[Brief Description of the Drawings]

Fig. 1 is a cross-sectional view showing a semiconductor device of the present invention in which a copper interconnection and a capacitor are formed in the same layer.

Figs. 2a to 2g are cross-sectional views illustrating a method for forming a semiconductor device in accordance with an embodiment of the present invention.

Figs. 3a and 3b is a plane figure depicting a method for forming a semiconductor device in accordance with an embodiment of the present invention.

Fig. 4 is a cross-sectional view showing a method for forming a semiconductor device in accordance with a second embodiment of the present invention.

● Description of main symbols in Figures

100: first insulation layer

115: second insulation layer

125: third insulation layer

135: interconnection trench

140: via hole

145: first barrier metal

150: first copper interconnection

160: first electrode

165: dielectric layer

170: second electrode

175: second barrier metal

180: second copper interconnection

[Description of Invention]

[Purpose of Invention]

[Field of the Invention and Description of Related Art]

The present invention relates to a method for fabricating a semiconductor device; and, more particularly, to a semiconductor device with a capacitor and an interconnection formed by a damascene process.

Logic elements become more highly integrated and their processing speed gets faster and faster, as transistors become finer. In response to the integration of transistors, interconnections have become finer and the number of interconnection layers is increasing drastically. As a result, a matter of interconnection delay caused by the miniaturization is intensified in a high-speed and highly integrated device as a factor that obstructs a device to become faster.

In this circumstance, a method of forming an interconnection using copper (Cu) with a lower specific resistance and higher EM (electromigration) property than an aluminum alloy, a material conventionally used for the

interconnections of a LSI (large scale integration).

However, since copper is not easily etched in a conventional dry etching method which has been used for forming an aluminum interconnection, and it is oxidized during the process, a damascene process is used to form a copper interconnection.

The damascene process is entirely different from a conventional processing series of ① an aluminum deposition, ② reactive ion etching (RIE) and ② deposition of insulation material and planarization. That is, the damascene process is a filling process composed of forming an interconnection trench and a via hole on an insulation layer, filling them with copper and planarizing it in a chemical mechanical polishing (hereinafter, referred to CMP) method.

There are a single damascene process which forms an interconnection trench and via plug separately and a dual damascene process which forms the via plug and interconnection trench concurrently. In case of the dual damascene process, since the via plug and interconnection trench are formed concurrently, the aspect ratio is higher than the single damascene process, but the dual damascene process is commonly used from a point view of lowering process cost.

The dual damascene process consists of a series of ① forming a via hole and an interconnection trench, ② forming a barrier metal, ③ filling the via hole and interconnection trench with copper and ④ polishing the copper and the barrier

metal in a CMP method.

Meanwhile, a capacitor, a passive element, is formed in the process of a semiconductor device fabrication to form various logic elements. As an example, in a MPU (micro processor unit), a decoupling capacitor is formed; and in a SOC (system on a chip) and a radio frequency (RF) element, a coupling and bypass capacitor is formed for impedance matching between the blocks, while in an AD (analog to digital) or a DA (digital to analog), a capacitor array is formed.

To form these capacitors, a junction capacitor using a silicon junction or as a technique using a conventional aluminum, a metal/insulator/metal (MIM) capacitor of aluminum/silicon nitride layer/aluminum (Al/SiN/Al) that is formed by using a silicon nitride (SiN) layer as a dielectric layer which is deposited in a plasma enhanced chemical vapor deposition (hereinafter, referred to PECVD) method, has been formed so far.

However, as operation frequency and bit of converter increase, a capacitor with higher capacity comes to be needed. For instance, in case of a CPU (central processing unit) that operates at 1GHz, 400nF of capacitor capacity is needed for decoupling. Here, if the thickness (Toxeq) of an effective oxide layer is 1nm, the capacitor is 34.5 nF/mm^2, and after all an area of 11.6mm^2 is needed for 400nF. The dielectric constant of a 1000Å SiN layer deposited in a PECVD method is 7, the thickness (Toxeq) of an effective oxide layer is around 56nm, and as the capacitance is 0.62 nF/mm^2, a capacitor with

an area of 645mm^2 is needed for 400nF, which cannot be realized in the conventional manufacturing of a semiconductor chip.

Consequently, a structure that can increase the capacity of a capacity without increasing the processing steps and the area of a device is required.

[Technical object achieved by Invention]

It is, therefore, an object of the present invention to provide a method for fabricating a semiconductor device that forms a capacitor and a metal interconnection in the same level of a layer by using a damascene process method, and a semiconductor device formed by the method.

[Detailed Description of Invention]

In accordance with an embodiment of the present invention, there is provided a method for forming a semiconductor device, including the steps of: a) forming an insulation layer in a capacitor region and a metal interconnection region on a substrate; b) forming a metal interconnection at the metal interconnection region of the insulation layer by performing a dual damascene process; and c) forming a capacitor in the same layer as the metal interconnection in the insulation layer of the capacitor region.

In accordance with an embodiment of the present invention, there is provided a method for fabricating a semiconductor device, comprising the steps of: a) forming an insulation

layer including a first and a second insulation layers in the capacitor region and the metal interconnection region on a substrate formed with a lower conductive layer; b) forming an interconnection trench in the metal insulation region, a first trench in the capacitor region and a via hole connected to the lower conductive layer by selectively etching the insulation layer; c) forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them; d) forming a second trench by selectively forming the second insulation layer of the capacitor region; e) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench; and f) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

In accordance with an embodiment of the present invention, there is provided a method for fabricating a semiconductor device, comprising the steps of: a) forming an insulation layer including a first and a second insulation layers in the metal interconnection region and the capacitor region on the substrate formed with a lower conductive layer; b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer; c) forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first

copper layer in the interconnection trench, the via hole and the first trench and planarizing them; d) forming a second trench by selectively etching the second insulation layer around the first copper interconnection in the capacitor region; e) forming a third trench in the first barrier metal by selectively etching the first copper interconnection; f) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches; and g) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

In accordance with an embodiment of the present invention, there is provided a semiconductor device, comprising: a substrate; an insulation layer formed in the metal interconnection region and the capacitor region on the substrate; a metal interconnection in the insulation layer of the metal interconnection; and a capacitor formed in the same layer as the metal interconnection in the capacitor region of the insulation layer.

The present invention forms a three-dimensional capacitor on a damascene pattern by maintaining the conventional process in a damascene process. That is, it is a method fabricating a capacitor that can proceed with a damascene interconnection process, and there is no increase in the number of layers.

This invention separates a region for forming a meal interconnection and a region for forming a capacitor by the damascene process, and in a region for a capacitor, a separate

procedure is carried out to form the metal interconnection and the capacitor in the same level of a layer.

Above mentioned objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, which is set forth hereinafter.

Fig. 1 is a cross-sectional view showing a semiconductor device in which copper intersections and a capacitor is formed concurrently in a damascene process in accordance with an embodiment of the present invention, and Fig. 3A is a plane figure of Fig. 1. Fig. 1 is a cross-section cut out along the line k to k' of the semiconductor device of Fig. 3A.

In the drawing, there are a lower insulation layer (100) and a lower interconnection (105), and on top of them, a copper anti-diffusion insulation layer (110), a first insulation layer (115) formed with via holes, an etching blocking layer (120), a second insulation layer (125) and a hard mask layer (130) are deposited.

Within the second insulation layer (125), a capacitor in a winding shape and an interconnection are formed in the capacitor region (A) of same layer and a metal interconnection region, respectively, by a damascene process.

As illustrated in Fig. 1, the capacitor region (A) includes a first copper interconnection (150), a first electrode (160), a dielectric layer (165), a capacitor (172) formed with a second electrode (170) at the side and the bottom surfaces of a trench formed between the first copper

interconnection (150), and a second copper interconnection (180) connected to the second electrode (170). Preferably, a first barrier metal (145) is formed between the first electrode (160) and the first copper interconnection (150), and a second barrier metal (175) is formed between the second electrode (170) and the second copper interconnection (180).

The metal interconnection region (B) is formed by a conventional dual damascene process, as described in Fig. 1, and there is a metal interconnection (152) formed between the second inter-layer dielectric layer (125).

To describe the plane figure of a capacitor in the capacitor region (A) with reference to Fig. 3a, a first electrode, a capacitor consists of a dielectric layer and a second electrode is formed between the winding-shaped first copper interconnection (150) and the second copper interconnection (180). The capacitor (172) is formed of a first electrode, a dielectric layer and a second electrode deposited in order, although they are not illustrated in the drawing. Also, although not illustrated, a first and a second barrier metals are formed between the capacitor and the first and the second copper interconnection.

In the metal interconnection region (B), the copper interconnection (152) formed by a damascene process are disposed at regular intervals with an insulation layer (125B). In the plane figure of Fig. 3a, a via contact connected between the interconnection is not illustrated.

The first and the second insulation layers (115, 125)

uses at least one selected from SiO_2, SiOC, SiOH, SiOCH and insulation layers with low dielectric constants below 3.0. Insulation layers with low dielectric constants (low-k) decrease the parasitic capacity between the copper interconnection and interconnection resistance along with a copper interconnection and make the speed of a device fast, and it is known as an alternative that can reduce cross talk of a device. Various insulation layers with low dielectric constants (low-k) are under development, and largely they are classified into two groups: a SiO_2 group (Si-O group) and a carbon group (C group). The SiO_2 group includes FSG (fluorine-doped silicate glass), HSQ (hydrogen silsesquioxane), SOG (inorganic spin on glass), organic SOG, etc, while the carbon group polymers are classified according to the presence of fluorine F.

The anti-diffusion layer (110), etching blocking layer (120) and hard mask (130) use SiN, SiC and SiCN layer at a thickness of 100Å to 1000Å. Here, the etching blocking layer and the hard mask can be omitted according to a dual damascene patterning method and the kind of used layers. Also, the hard mask (130) can be formed dual top hard mask.

The barrier metals (145, 175) uses one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN and a combination thereof.

The dielectric layer (165) of the capacitor uses one selected from a group of Ta oxides, Ba-Sr-Ti oxides, Zr oxides, Hf oxides, Pb-Zn-Ti oxides and Sr-Bi-Ta oxides and a

combination thereof.

As the first and the second electrodes (160, 170) of the capacitor, a metal such as Pt, Ru, Ir and W is used. Preferably, when forming a lower electrode conductive layer, a lower electrode conductive layer is deposited after an adhesive layer of TiN, TiAlN and TiSiN is formed to enhance the adhesiveness of the insulation layer in the lower part.

Copper damascene has been described in the above embodiment, but the interconnections and capacitors can be formed on an oxide metal or a conductive compound other conductive metals other than copper.

Figs. 2a to 2g shows a method for forming the structure of Fig. 1.

Fig. 2a is a cross-sectional view showing a method of forming a series of insulation layers on the lower insulation layer (100) in which a lower interconnection (105) is formed in accordance with the present invention.

There are a lower insulation layer (100) and a lower interconnection (105), and on top of them, a copper anti-diffusion insulation layer (110), a first insulation layer (115), an etching blocking layer (120), a second insulation layer (125) and a hard mask layer (130) are deposited in order. The first insulation layer (115) is a part where a via connecting an upper and lower copper interconnections is to be formed later, while the second insulation layer (125) is a part where a copper interconnection and a capacitor are formed in the same layer.

The first insulation layer (115) and the second insulation layer (125) use at least one selected from SiO_2, SiOC, SiOH, SiOCH and insulation layers with low dielectric constants below 3.0. As a deposition method, a PECVD, a HDP-CVD (high density plasma CVD), an APCVD (atmospheric pressure CVD), or a spin coating method is used.

As the copper anti-diffusion layer (110), the etching blocking layer (120) and the hard mask (130), a SiN, SiC, SiCN layer deposited in the PECVD method is used at a thickness of 100Å to 1000Å.

Fig. 2b is a cross-sectional view illustrating a method for forming an interconnection trench, a winding-shaped first trench (136) and a via hole (140).

The method of forming a dual damascene includes a via first method where a via hole is formed first prior to an interconnection trench, a trench first method where an interconnection trench is formed first prior to a via hole and so forth.

The interconnection trench (135) and the first trench (136) are formed in the same layer concurrently, but their roles are different. That is, a copper interconnection is to be formed later in the interconnection trench (135), while a first copper interconnection to be connected to an electrode of a capacitor is formed in the first trench (136) in the same insulation layer.

Fig. 3b is a plane figure and Fig. 2b is a cross-sectional view of a semiconductor device of Fig. 3b cut out

along the line t to t'. In the metal interconnection region B, the interconnection trench (135) where a copper interconnection later is to be formed is a line located in a predetermined gap between the second insulation layers (125b), but is connected planarily to the first trench (136) where a winding-shaped first copper interconnection to be connected to an electrode of a capacitor is to be formed in the capacitor region (A). The insulation layer is divided to a capacitor region (125b) and a metal interconnection region (125a) in an insulation layer, for convenience. The winding shape can be transformed into various crookednesses and shapes other than the structure shown in Fig. 3b.

Fig. 2C is a cross-sectional view showing a copper interconnection (152) and a first copper interconnection (150) by a damascene process in accordance with the present invention.

First, a first barrier metal (145) is formed on the entire surface of a substrate formed with the interconnection trench (135), winding-shaped first trench (136) and via hole (140). The first barrier metal (145) is used to prevent the deterioration in the electric property of a capacitor and in the insulation property of an inter-layer dielectric layer by the diffusion of a copper conductive material formed later on. The first barrier metal uses one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN and a combination thereof as its material. As a deposition method, a physical vapor deposition (hereinafter, referred to PVD), a chemical

vapor deposition (hereinafter, referred to CVD) or an atomic layer deposition (hereinafter, referred to ALD) method is used.

Preferably, a cleansing procedure is performed to make fine the conditions of the interface between the lower interconnection and via bottom, and the interface between the metal surface and the inter-layer dielectric layer before the deposition of the first barrier metal (145) to make resistance low. This is because copper oxide becomes the cause for increasing a via resistance when it remains at the via bottom, and also the copper in the oxide layer is diffused when it remains in the inter-layer dielectric layer. The cleaning step includes the steps of: loading a wafer in a deposition equipment; performing degas in a high pressure vacuum condition; and performing an Ar sputter cleaning or a reactive cleaning using a plasma containing hydrogen such as H_2, NH_3, etc.

Subsequently, a first copper layer is formed on the substrate. Here, the first copper layer is formed to fill up the interconnection trench (135), the first trench (136) and the via hole (140). The first copper layer is formed in the reflow method after forming the layer din the sputtering method, the CVD method or an electroplating method.

In case of using the electroplating method, a seed layer needs to be formed on top of the first barrier metal (145) to flow a current during electrolysis. That is, the first copper conducive layer can be formed by the electroplating method after forming a copper seed layer in the PVD or CVD method,

after forming a seed layer in an electroless deposition or a combination thereof.

After the formation of the first conductive layer, the first copper conductive layer and the first barrier metal on the insulation layer are removed by carrying out the planarization until the insulation layer is exposed using the CMP. Accordingly, in the capacitor region (A), a winding-shaped first copper interconnection (150) is formed, and in the metal interconnection region, a copper interconnection (152) is formed.

Fig. 2d is a cross-sectional view of a method photoreist pattern (155) formed to expose the capacitor region (A) in accordance with the present invention.

The exposed region is a capacitor region (A) where the winding-shaped capacitor is to be formed, and the metal interconnection region (B) is not exposed.

Fig. 2e is a cross-sectional view showing a method of forming a winding-shaped second trench (154) by selectively etching the second insulation layer (125) of the capacitor region (A) in accordance with the present invention.

The winding-shaped second trench (154) where a capacitor is to be formed later is formed by selectively etching the second insulation layer (125) of the capacitor region (A), using the photoresist pattern (155) formed above. With reference to Fig. 3b, the second insulation layer of a reference numeral '125A' is removed and a winding-shaped second trench (154) is formed thereon.

In case a hard mask layer (130) is used on top of the second insulation layer (125), the hard mask layer (130) is removed by performing a plasma dry etching with a gas including fluorine.

Subsequently, in case the second insulation layer 125 is formed of SiO_2, FSG, SiOC, SiOH and SiOCH, the second insulation layer 125 is removed by using a solution containing HF. If the second insulation layer (125) is a low-k insulation layer formed of a polymer, the second insulation layer (125) is removed by using O_2 plasma. While the second insulation layer is etched, the first insulation layer (115) is not damaged because there is an etching blocking layer (120) in the middle of the insulation layer.

Fig. 2f is a cross-sectional view showing a layer to be a capacitor and a second barrier metal in accordance with the present invention.

On the entire surface of the substrate, a first electrode (160), a dielectric layer (165) and a second electrode (170) are formed in order, and then a second barrier metal (175) is formed.

As the first and second electrodes (160, 170), a metal such as Pt, Ru, Ir and W is used, and as for a deposition method, the CVD, PVD or ALD method is used. Preferably, when a lower electrode conductive layer is formed, an adhesive layer of TiN, TiAlN, TiSiN, etc is formed to make good the adhesiveness with the lower insulation layer and then a first electrode (160) is deposited.

As for a dielectric layer (165) of the capacitor, Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide or Sr-Bi-Ta oxide is used. As for a deposition method, the CVD, PVD or ALD method is used.

The second barrier metal (175) is used to prevent the deterioration in the electric property of a capacitor and the insulation property of an inter-layer insulation layer.

Before the deposition of the second barrier metal (175), a wafer is loaded in a deposition equipment. Degas process is performed in a high pressure vacuum condition; and an Ar sputter cleaning or a reactive cleaning using a plasma containing hydrogen such as H_2, NH_3, etc is used. The material and cleaning method of the second barrier metal is the same as those of the first barrier metal described above.

Fig. 2g is a cross-sectional view illustrating a second copper layer in accordance with the present invention.

On the entire surface of the substrate, a second copper layer (180) is formed. Here, the second copper layer (180) fills up the substrate entirely. The method of forming the second copper layer (180) is the same as that of the first copper layer described above.

Subsequently, when the second copper layer (180) is planarized, it becomes a semiconductor device formed with a capacitor and a copper interconnection as shown in Figs. 1 and 3A.

The planarization proceeds until the first copper interconnection (150) and the copper interconnection (152) are

exposed by using the CMP. That is, a capacitor whose side and bottom surfaces become the effective area of the capacitor is formed in the capacitor region (A) and the copper interconnection (B) is formed in the metal interconnection region B by removing a second copper layer, a second barrier metal, a first electrode, a dielectric layer and a second electrode on top of the first copper interconnection (150) and the copper interconnection (152).

Subsequently, as illustrated in Fig. 1, after the procedures of forming the capacitor and the copper interconnection, the inter-layer dielectric layers of a series of a copper anti-diffusion insulation layer, a second insulation layer, an etching blocking layer, a third insulation layer and a hard mask layer are deposited in order to form another multiplayer interconnection. After that, a via hole, an interconnection trench or, if necessary, a winding-shaped trench is formed and a multiplayer interconnection process proceeds.

Fig. 4 shows a second embodiment of the present invention, whose process is the same as that of Figs. 2a to 2e.

The difference is that a process of Fig. 4 is performed after the process from Figs. 2a to 2e.

To briefly describe it, a series of insulation layers including a copper anti-diffusion layer (410), a first insulation layer (415), an etching blocking layer (420), a second insulation layer (425) and a hard mask (430) are formed on the lower insulation layer (400) formed with a copper lower

interconnection (405), and an interconnection trench, a winding-shaped first trench and a via hole are formed. Subsequently, a first barrier metal (445) is deposited, and a copper interconnection (452) in the interconnection trench, a first copper interconnection in the first trench and a via contact plug are formed. Subsequently, a photoresist pattern is formed to expose the region to be formed with a capacitor later, a winding-shaped second trench (454) is formed by using the photoresist pattern and removing the exposed second insulation layer.

The subsequent processes are different from the first embodiment. A winding-shaped third trench (456) is formed in the first barrier metal by removing the first copper interconnection of the capacitor region (A).

Fig. 4 is a cross-sectional view showing a second insulation layer (425) of the capacitor region (A) where a first copper interconnection is removed. In the region where the second insulation layer is removed, a second trench (454) is formed and in the region where the first copper interconnection is removed, a third trench (456) is formed.

Since the first copper interconnection needs to be etched in the capacitor region (A) only, a photo process is performed so that the copper interconnection in the metal interconnection region (B) should not be damaged. A three-dimensional structure of the first barrier metal (445) is formed by removing the second insulation layer and the first copper interconnection, as shown in Fig. 4. Then, HCl or H_2SO_4

acid solution is used to etch the first copper interconnection only without damaging the first barrier metal.

After the formation of a three-dimensional structure of the first barrier metal (445) only, the process same as the processing order of the first embodiment in Figs. 2f and 2g is performed. That is, a first electrode, a dielectric layer and a second electrode are formed to form a capacitor. Subsequently, a second barrier metal is deposited, and after the deposition of a second copper conductive layer, a capacitor is formed in the same layer as the copper interconnection by performing the CMP.

Therefore, the second embodiment is proceeded in the same processing as those in Figs. 2a to 2e of the first embodiment, and a process of Fig. 4 that removes the first copper conductive layer in HCl or H_2SO_4 acid solution is added.

In the second embodiment, a first barrier metal is formed in a winding shape, and the second copper interconnection and the capacitor are formed at what is supposed to be a part for an insulation layer and a part for the first copper interconnection conventionally. That is, with the first barrier metal in the center, a capacitor composed of a first electrode on both sides and at the bottom, a dielectric layer, a second electrode, a second barrier metal and a second copper interconnection is formed.

In other words, the semiconductor including the capacitor comprises: a barrier metal with a winding-shaped first trench (the winding-shaped third trench) inside; a second trench (a

winding-shaped second trench) formed between the barrier metal; and a capacitor formed with a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the first and the second trenches.

Compared to the first embodiment, the second embodiment has an advantage that the capacitor area increases further.

The above embodiment describes about a copper damascene, but the same interconnection process can be performed in the other conductive metal, oxide metal or conductive compounds other than copper, and the same capacitor can be formed.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.

[Effect of Invention]

The present invention described above forms a capacitor without increasing the number of processing steps by fabricating a capacitor in the same layer as the metal interconnection, maintaining the damascene process for forming a conventional interconnection.

Also, the structure of the capacitor can be embodied easily by the damascene process, thus obtaining a capacitance of high capacity which is needed for logic elements.

[Claims]

1. A method for forming a semiconductor device, comprising the steps of:

forming an insulation layer in a capacitor region and a metal interconnection region on a substrate;

forming a metal interconnection at the metal interconnection region of the insulation layer by performing a dual damascene process; and

forming a capacitor in the same layer as the metal interconnection in the insulation layer of the capacitor region.

2. The method as recited in claim 1, wherein the forming a capacitor includes the steps of:

forming a first trench at the capacitor region of the insulation layer;

forming a first metal interconnection inside the first trench;

forming a second trench by removing the insulation layer between the first metal interconnection; and

forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench.

3. The method as recited in claim 1, wherein the forming a capacitor includes the steps of:

forming a first trench in the capacitor region of the insulation layer;

forming a first barrier metal and a first metal interconnection inside the first trench;

forming a second trench by removing the insulation layer around the first barrier metal;

forming a third trench in the first barrier metal by removing the first metal interconnection; and

forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches.

4. The method as recited in claim 2 or 3, further comprising the step of forming a second metal interconnection connected to the second electrode of the capacitor.

5. The method as recited in claim 2 or 3, wherein the first metal interconnection is of copper.

6. The method as recited in claim 2 or 3, wherein the first and the second electrodes are of a metal selected from a group of Pt, Ru, Ir and W.

7. The method as recited in claim 2 or 3, wherein the dielectric layer is of an oxide selected from a group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.

8. A method for fabricating a semiconductor device, comprising the steps of:

forming an insulation layer including a first and a second insulation layers in the capacitor region and the metal interconnection region on a substrate formed with a lower conductive layer;

forming an interconnection trench in the metal insulation region, a first trench in the capacitor region and a via hole connected to the lower conductive layer by selectively etching the insulation layer;

forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them;

forming a second trench by selectively forming the second insulation layer of the capacitor region;

forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench; and

forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

9. A method for fabricating a semiconductor device, comprising the steps of:

a) forming an insulation layer including a first and a second insulation layers in the metal interconnection region

and the capacitor region on the substrate formed with a lower conductive layer;

b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer;

c) forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them;

d) forming a second trench by selectively etching the second insulation layer around the first copper interconnection in the capacitor region;

e) forming a third trench in the first barrier metal by selectively etching the first copper interconnection;

f) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches; and

g) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

10. The method as recited in claim 8 or 9, wherein the insulation layer includes an etching blocking layer between the first insulation layer and the second insulation layer.

11. The method as recited in claim 8 or 9, further including a hard mask on the second insulation layer.

12. The method as recited in claim 8 or 9, wherein the forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer forms the interconnection trench and the first trench simultaneously first, and then forming the via hole.

13. The method as recited in claim 8 or 9, wherein the forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer forms the via hole first, and then forming the interconnection trench and the first trench simultaneously.

14. The method as recited in claim 8 or 9, wherein the first and the second copper conductive layers use a reflow method after forming a layer in a sputtering method, a CVD method or an electroplating method.

15. The method as recited in claim 14, wherein in case of using the electroplating method, a seed layer is formed in a method selected from a group of a physical vapor deposition (PVD), a chemical vapor deposition (CVD) and an electroless deposition, or a combination thereof.

16. The method as recited in claim 8, further including the steps of:

g) forming a first barrier metal prior to the first copper layer; and

h) forming a second barrier metal prior to the second copper layer.

17. The method as recited in claim 9, wherein a second barrier metal is formed prior to the formation of the second copper layer.

18. The method as recited in claim 9, 16 or 17, wherein the first and the second barrier metals is of one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN, and a combination thereof.

19. A semiconductor device, comprising:

a substrate;

an insulation layer formed in the metal interconnection region and the capacitor region on the substrate;

a metal interconnection in the insulation layer of the metal interconnection; and

a capacitor formed in the same layer as the metal interconnection in the capacitor region of the insulation layer.

20. The semiconductor device as recited in claim 19, wherein the capacitor includes:

a first metal interconnection;

a trench formed between the first metal interconnection; and

a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the trench.

21. The semiconductor device as recited in claim 17, wherein the capacitor includes:

a barrier metal with a first trench inside;

a second trench formed between the barrier metal; and

a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the first and the second trench.

22. The semiconductor device as recited in claim 20 or 21, further including a second metal interconnection connected to the second electrode of the capacitor.

23. The semiconductor device as recited in claim 20 or 22, wherein the first and the second metal interconnections are formed by depositing the copper layer and the barrier metal.

24. The semiconductor device as recited in claim 19, wherein the insulation layer is of a material selected from a group of SiO_2, SiOC, SiOH, SiOCH, insulation layers with dielectric constants below 3.0, and a combination thereof.

25. The semiconductor device as recited in claim 20 or 21, wherein the dielectric layer is of an oxide selected from a

group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.

26. The semiconductor device as recited in claim 20, wherein the first and the second electrodes are of a metal selected from a group of Pt, Ru, Ir and W.

27. The semiconductor device as recited in claim 23, wherein the barrier metal is of a material selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN, TaSiN, and a combination thereof.

[Abstract of the Disclosure]

[Abstract]

The present invention relates to a method for fabricating a semiconductor device that forms a capacitor in the same level of a simultaneously in a damascene process, and this invention brings about the effect of obtaining a capacitance of a high capacity needed for logic elements without increasing the number of layers for fabricating a capacitor by forming a three-dimensional capacitor in the damascene pattern while maintaining the conventional processes in a damascene interconnection process.

[Representative Figure]

Figure 1

[Index]

Serpentine, Capacitor, Damascene, Copper, Via

[Specification]

[Title of Invention]

METHOD OF FORMING SEMICONDUCTOR DEVICE WITH CAPACITOR AND METAL-INTERCONNECTION IN DAMASCENE PROCESS

[Brief Description of the Drawings]

Fig. 1 is a cross-sectional view showing a semiconductor device of the present invention in which a copper interconnection and a capacitor are formed in the same layer.

Figs. 2a to 2g are cross-sectional views illustrating a method for forming a semiconductor device in accordance with an embodiment of the present invention.

Figs. 3a and 3b is a plane figure depicting a method for forming a semiconductor device in accordance with an embodiment of the present invention.

Fig. 4 is a cross-sectional view showing a method for forming a semiconductor device in accordance with a second embodiment of the present invention.

● Description of main symbols in Figures

100: first insulation layer

115: second insulation layer

125: third insulation layer

135: interconnection trench

140: via hole

145: first barrier metal

150: first copper interconnection

160: first electrode

165: dielectric layer

170: second electrode

175: second barrier metal

180: second copper interconnection

[Description of Invention]

[Purpose of Invention]

[Field of the Invention and Description of Related Art]

The present invention relates to a method for fabricating a semiconductor device; and, more particularly, to a semiconductor device with a capacitor and an interconnection formed by a damascene process.

Logic elements become more highly integrated and their processing speed gets faster and faster, as transistors become finer. In response to the integration of transistors, interconnections have become finer and the number of interconnection layers is increasing drastically. As a result, a matter of interconnection delay caused by the miniaturization is intensified in a high-speed and highly integrated device as a factor that obstructs a device to become faster.

In this circumstance, a method of forming an interconnection using copper (Cu) with a lower specific resistance and higher EM (electromigration) property than an aluminum alloy, a material conventionally used for the

interconnections of a LSI (large scale integration).

However, since copper is not easily etched in a conventional dry etching method which has been used for forming an aluminum interconnection, and it is oxidized during the process, a damascene process is used to form a copper interconnection.

The damascene process is entirely different from a conventional processing series of ① an aluminum deposition, ② reactive ion etching (RIE) and ② deposition of insulation material and planarization. That is, the damascene process is a filling process composed of forming an interconnection trench and a via hole on an insulation layer, filling them with copper and planarizing it in a chemical mechanical polishing (hereinafter, referred to CMP) method.

There are a single damascene process which forms an interconnection trench and via plug separately and a dual damascene process which forms the via plug and interconnection trench concurrently. In case of the dual damascene process, since the via plug and interconnection trench are formed concurrently, the aspect ratio is higher than the single damascene process, but the dual damascene process is commonly used from a point view of lowering process cost.

The dual damascene process consists of a series of ① forming a via hole and an interconnection trench, ② forming a barrier metal, ③ filling the via hole and interconnection trench with copper and ④ polishing the copper and the barrier

metal in a CMP method.

Meanwhile, a capacitor, a passive element, is formed in the process of a semiconductor device fabrication to form various logic elements. As an example, in a MPU (micro processor unit), a decoupling capacitor is formed; and in a SOC (system on a chip) and a radio frequency (RF) element, a coupling and bypass capacitor is formed for impedance matching between the blocks, while in an AD (analog to digital) or a DA (digital to analog), a capacitor array is formed.

To form these capacitors, a junction capacitor using a silicon junction or as a technique using a conventional aluminum, a metal/insulator/metal (MIM) capacitor of aluminum/silicon nitride layer/aluminum (Al/SiN/Al) that is formed by using a silicon nitride (SiN) layer as a dielectric layer which is deposited in a plasma enhanced chemical vapor deposition (hereinafter, referred to PECVD) method, has been formed so far.

However, as operation frequency and bit of converter increase, a capacitor with higher capacity comes to be needed. For instance, in case of a CPU (central processing unit) that operates at 1GHz, 400nF of capacitor capacity is needed for decoupling. Here, if the thickness (Toxeq) of an effective oxide layer is 1nm, the capacitor is 34.5 nF/mm^2, and after all an area of 11.6mm^2 is needed for 400nF. The dielectric constant of a 1000Å SiN layer deposited in a PECVD method is 7, the thickness (Toxeq) of an effective oxide layer is around 56nm, and as the capacitance is 0.62 nF/mm^2, a capacitor with

an area of 645mm^2 is needed for 400nF, which cannot be realized in the conventional manufacturing of a semiconductor chip.

Consequently, a structure that can increase the capacity of a capacity without increasing the processing steps and the area of a device is required.

[Technical object achieved by Invention]

It is, therefore, an object of the present invention to provide a method for fabricating a semiconductor device that forms a capacitor and a metal interconnection in the same level of a layer by using a damascene process method, and a semiconductor device formed by the method.

[Detailed Description of Invention]

In accordance with an embodiment of the present invention, there is provided a method for forming a semiconductor device, including the steps of: a) forming an insulation layer in a capacitor region and a metal interconnection region on a substrate; b) forming a metal interconnection at the metal interconnection region of the insulation layer by performing a dual damascene process; and c) forming a capacitor in the same layer as the metal interconnection in the insulation layer of the capacitor region.

In accordance with an embodiment of the present invention, there is provided a method for fabricating a semiconductor device, comprising the steps of: a) forming an insulation

layer including a first and a second insulation layers in the capacitor region and the metal interconnection region on a substrate formed with a lower conductive layer; b) forming an interconnection trench in the metal insulation region, a first trench in the capacitor region and a via hole connected to the lower conductive layer by selectively etching the insulation layer; c) forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them; d) forming a second trench by selectively forming the second insulation layer of the capacitor region; e) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench; and f) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

In accordance with an embodiment of the present invention, there is provided a method for fabricating a semiconductor device, comprising the steps of: a) forming an insulation layer including a first and a second insulation layers in the metal interconnection region and the capacitor region on the substrate formed with a lower conductive layer; b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer; c) forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first

copper layer in the interconnection trench, the via hole and the first trench and planarizing them; d) forming a second trench by selectively etching the second insulation layer around the first copper interconnection in the capacitor region; e) forming a third trench in the first barrier metal by selectively etching the first copper interconnection; f) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches; and g) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

In accordance with an embodiment of the present invention, there is provided a semiconductor device, comprising: a substrate; an insulation layer formed in the metal interconnection region and the capacitor region on the substrate; a metal interconnection in the insulation layer of the metal interconnection; and a capacitor formed in the same layer as the metal interconnection in the capacitor region of the insulation layer.

The present invention forms a three-dimensional capacitor on a damascene pattern by maintaining the conventional process in a damascene process. That is, it is a method fabricating a capacitor that can proceed with a damascene interconnection process, and there is no increase in the number of layers.

This invention separates a region for forming a meal interconnection and a region for forming a capacitor by the damascene process, and in a region for a capacitor, a separate

procedure is carried out to form the metal interconnection and the capacitor in the same level of a layer.

Above mentioned objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, which is set forth hereinafter.

Fig. 1 is a cross-sectional view showing a semiconductor device in which copper intersections and a capacitor is formed concurrently in a damascene process in accordance with an embodiment of the present invention, and Fig. 3A is a plane figure of Fig. 1. Fig. 1 is a cross-section cut out along the line k to k' of the semiconductor device of Fig. 3A.

In the drawing, there are a lower insulation layer (100) and a lower interconnection (105), and on top of them, a copper anti-diffusion insulation layer (110), a first insulation layer (115) formed with via holes, an etching blocking layer (120), a second insulation layer (125) and a hard mask layer (130) are deposited.

Within the second insulation layer (125), a capacitor in a winding shape and an interconnection are formed in the capacitor region (A) of same layer and a metal interconnection region, respectively, by a damascene process.

As illustrated in Fig. 1, the capacitor region (A) includes a first copper interconnection (150), a first electrode (160), a dielectric layer (165), a capacitor (172) formed with a second electrode (170) at the side and the bottom surfaces of a trench formed between the first copper

interconnection (150), and a second copper interconnection (180) connected to the second electrode (170). Preferably, a first barrier metal (145) is formed between the first electrode (160) and the first copper interconnection (150), and a second barrier metal (175) is formed between the second electrode (170) and the second copper interconnection (180).

The metal interconnection region (B) is formed by a conventional dual damascene process, as described in Fig. 1, and there is a metal interconnection (152) formed between the second inter-layer dielectric layer (125).

To describe the plane figure of a capacitor in the capacitor region (A) with reference to Fig. 3a, a first electrode, a capacitor consists of a dielectric layer and a second electrode is formed between the winding-shaped first copper interconnection (150) and the second copper interconnection (180). The capacitor (172) is formed of a first electrode, a dielectric layer and a second electrode deposited in order, although they are not illustrated in the drawing. Also, although not illustrated, a first and a second barrier metals are formed between the capacitor and the first and the second copper interconnection.

In the metal interconnection region (B), the copper interconnection (152) formed by a damascene process are disposed at regular intervals with an insulation layer (125B). In the plane figure of Fig. 3a, a via contact connected between the interconnection is not illustrated.

The first and the second insulation layers (115, 125)

uses at least one selected from SiO_2, SiOC, SiOH, SiOCH and insulation layers with low dielectric constants below 3.0. Insulation layers with low dielectric constants (low-k) decrease the parasitic capacity between the copper interconnection and interconnection resistance along with a copper interconnection and make the speed of a device fast, and it is known as an alternative that can reduce cross talk of a device. Various insulation layers with low dielectric constants (low-k) are under development, and largely they are classified into two groups: a SiO_2 group (Si-O group) and a carbon group (C group). The SiO_2 group includes FSG (fluorine-doped silicate glass), HSQ (hydrogen silsesquioxane), SOG (inorganic spin on glass), organic SOG, etc, while the carbon group polymers are classified according to the presence of fluorine F.

The anti-diffusion layer (110), etching blocking layer (120) and hard mask (130) use SiN, SiC and SiCN layer at a thickness of 100Å to 1000Å. Here, the etching blocking layer and the hard mask can be omitted according to a dual damascene patterning method and the kind of used layers. Also, the hard mask (130) can be formed dual top hard mask.

The barrier metals (145, 175) uses one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN and a combination thereof.

The dielectric layer (165) of the capacitor uses one selected from a group of Ta oxides, Ba-Sr-Ti oxides, Zr oxides, Hf oxides, Pb-Zn-Ti oxides and Sr-Bi-Ta oxides and a

combination thereof.

As the first and the second electrodes (160, 170) of the capacitor, a metal such as Pt, Ru, Ir and W is used. Preferably, when forming a lower electrode conductive layer, a lower electrode conductive layer is deposited after an adhesive layer of TiN, TiAlN and TiSiN is formed to enhance the adhesiveness of the insulation layer in the lower part.

Copper damascene has been described in the above embodiment, but the interconnections and capacitors can be formed on an oxide metal or a conductive compound other conductive metals other than copper.

Figs. 2a to 2g shows a method for forming the structure of Fig. 1.

Fig. 2a is a cross-sectional view showing a method of forming a series of insulation layers on the lower insulation layer (100) in which a lower interconnection (105) is formed in accordance with the present invention.

There are a lower insulation layer (100) and a lower interconnection (105), and on top of them, a copper anti-diffusion insulation layer (110), a first insulation layer (115), an etching blocking layer (120), a second insulation layer (125) and a hard mask layer (130) are deposited in order. The first insulation layer (115) is a part where a via connecting an upper and lower copper interconnections is to be formed later, while the second insulation layer (125) is a part where a copper interconnection and a capacitor are formed in the same layer.

The first insulation layer (115) and the second insulation layer (125) use at least one selected from SiO_2, SiOC, SiOH, SiOCH and insulation layers with low dielectric constants below 3.0. As a deposition method, a PECVD, a HDP-CVD (high density plasma CVD), an APCVD (atmospheric pressure CVD), or a spin coating method is used.

As the copper anti-diffusion layer (110), the etching blocking layer (120) and the hard mask (130), a SiN, SiC, SiCN layer deposited in the PECVD method is used at a thickness of 100Å to 1000Å.

Fig. 2b is a cross-sectional view illustrating a method for forming an interconnection trench, a winding-shaped first trench (136) and a via hole (140).

The method of forming a dual damascene includes a via first method where a via hole is formed first prior to an interconnection trench, a trench first method where an interconnection trench is formed first prior to a via hole and so forth.

The interconnection trench (135) and the first trench (136) are formed in the same layer concurrently, but their roles are different. That is, a copper interconnection is to be formed later in the interconnection trench (135), while a first copper interconnection to be connected to an electrode of a capacitor is formed in the first trench (136) in the same insulation layer.

Fig. 3b is a plane figure and Fig. 2b is a cross-sectional view of a semiconductor device of Fig. 3b cut out

along the line t to t'. In the metal interconnection region B, the interconnection trench (135) where a copper interconnection later is to be formed is a line located in a predetermined gap between the second insulation layers (125b), but is connected planarily to the first trench (136) where a winding-shaped first copper interconnection to be connected to an electrode of a capacitor is to be formed in the capacitor region (A). The insulation layer is divided to a capacitor region (125b) and a metal interconnection region (125a) in an insulation layer, for convenience. The winding shape can be transformed into various crookednesses and shapes other than the structure shown in Fig. 3b.

Fig. 2C is a cross-sectional view showing a copper interconnection (152) and a first copper interconnection (150) by a damascene process in accordance with the present invention.

First, a first barrier metal (145) is formed on the entire surface of a substrate formed with the interconnection trench (135), winding-shaped first trench (136) and via hole (140). The first barrier metal (145) is used to prevent the deterioration in the electric property of a capacitor and in the insulation property of an inter-layer dielectric layer by the diffusion of a copper conductive material formed later on. The first barrier metal uses one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN and a combination thereof as its material. As a deposition method, a physical vapor deposition (hereinafter, referred to PVD), a chemical

vapor deposition (hereinafter, referred to CVD) or an atomic layer deposition (hereinafter, referred to ALD) method is used.

Preferably, a cleansing procedure is performed to make fine the conditions of the interface between the lower interconnection and via bottom, and the interface between the metal surface and the inter-layer dielectric layer before the deposition of the first barrier metal (145) to make resistance low. This is because copper oxide becomes the cause for increasing a via resistance when it remains at the via bottom, and also the copper in the oxide layer is diffused when it remains in the inter-layer dielectric layer. The cleaning step includes the steps of: loading a wafer in a deposition equipment; performing degas in a high pressure vacuum condition; and performing an Ar sputter cleaning or a reactive cleaning using a plasma containing hydrogen such as H_2, NH_3, etc.

Subsequently, a first copper layer is formed on the substrate. Here, the first copper layer is formed to fill up the interconnection trench (135), the first trench (136) and the via hole (140). The first copper layer is formed in the reflow method after forming the layer din the sputtering method, the CVD method or an electroplating method.

In case of using the electroplating method, a seed layer needs to be formed on top of the first barrier metal (145) to flow a current during electrolysis. That is, the first copper conducive layer can be formed by the electroplating method after forming a copper seed layer in the PVD or CVD method,

after forming a seed layer in an electroless deposition or a combination thereof.

After the formation of the first conductive layer, the first copper conductive layer and the first barrier metal on the insulation layer are removed by carrying out the planarization until the insulation layer is exposed using the CMP. Accordingly, in the capacitor region (A), a winding-shaped first copper interconnection (150) is formed, and in the metal interconnection region, a copper interconnection (152) is formed.

Fig. 2d is a cross-sectional view of a method photoreist pattern (155) formed to expose the capacitor region (A) in accordance with the present invention.

The exposed region is a capacitor region (A) where the winding-shaped capacitor is to be formed, and the metal interconnection region (B) is not exposed.

Fig. 2e is a cross-sectional view showing a method of forming a winding-shaped second trench (154) by selectively etching the second insulation layer (125) of the capacitor region (A) in accordance with the present invention.

The winding-shaped second trench (154) where a capacitor is to be formed later is formed by selectively etching the second insulation layer (125) of the capacitor region (A), using the photoresist pattern (155) formed above. With reference to Fig. 3b, the second insulation layer of a reference numeral '125A' is removed and a winding-shaped second trench (154) is formed thereon.

In case a hard mask layer (130) is used on top of the second insulation layer (125), the hard mask layer (130) is removed by performing a plasma dry etching with a gas including fluorine.

Subsequently, in case the second insulation layer 125 is formed of SiO_2, FSG, SiOC, SiOH and SiOCH, the second insulation layer 125 is removed by using a solution containing HF. If the second insulation layer (125) is a low-k insulation layer formed of a polymer, the second insulation layer (125) is removed by using O_2 plasma. While the second insulation layer is etched, the first insulation layer (115) is not damaged because there is an etching blocking layer (120) in the middle of the insulation layer.

Fig. 2f is a cross-sectional view showing a layer to be a capacitor and a second barrier metal in accordance with the present invention.

On the entire surface of the substrate, a first electrode (160), a dielectric layer (165) and a second electrode (170) are formed in order, and then a second barrier metal (175) is formed.

As the first and second electrodes (160, 170), a metal such as Pt, Ru, Ir and W is used, and as for a deposition method, the CVD, PVD or ALD method is used. Preferably, when a lower electrode conductive layer is formed, an adhesive layer of TiN, TiAlN, TiSiN, etc is formed to make good the adhesiveness with the lower insulation layer and then a first electrode (160) is deposited.

As for a dielectric layer (165) of the capacitor, Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide or Sr-Bi-Ta oxide is used. As for a deposition method, the CVD, PVD or ALD method is used.

The second barrier metal (175) is used to prevent the deterioration in the electric property of a capacitor and the insulation property of an inter-layer insulation layer.

Before the deposition of the second barrier metal (175), a wafer is loaded in a deposition equipment. Degas process is performed in a high pressure vacuum condition; and an Ar sputter cleaning or a reactive cleaning using a plasma containing hydrogen such as H_2, NH_3, etc is used. The material and cleaning method of the second barrier metal is the same as those of the first barrier metal described above.

Fig. 2g is a cross-sectional view illustrating a second copper layer in accordance with the present invention.

On the entire surface of the substrate, a second copper layer (180) is formed. Here, the second copper layer (180) fills up the substrate entirely. The method of forming the second copper layer (180) is the same as that of the first copper layer described above.

Subsequently, when the second copper layer (180) is planarized, it becomes a semiconductor device formed with a capacitor and a copper interconnection as shown in Figs. 1 and 3A.

The planarization proceeds until the first copper interconnection (150) and the copper interconnection (152) are

exposed by using the CMP. That is, a capacitor whose side and bottom surfaces become the effective area of the capacitor is formed in the capacitor region (A) and the copper interconnection (B) is formed in the metal interconnection region B by removing a second copper layer, a second barrier metal, a first electrode, a dielectric layer and a second electrode on top of the first copper interconnection (150) and the copper interconnection (152).

Subsequently, as illustrated in Fig. 1, after the procedures of forming the capacitor and the copper interconnection, the inter-layer dielectric layers of a series of a copper anti-diffusion insulation layer, a second insulation layer, an etching blocking layer, a third insulation layer and a hard mask layer are deposited in order to form another multiplayer interconnection. After that, a via hole, an interconnection trench or, if necessary, a winding-shaped trench is formed and a multiplayer interconnection process proceeds.

Fig. 4 shows a second embodiment of the present invention, whose process is the same as that of Figs. 2a to 2e.

The difference is that a process of Fig. 4 is performed after the process from Figs. 2a to 2e.

To briefly describe it, a series of insulation layers including a copper anti-diffusion layer (410), a first insulation layer (415), an etching blocking layer (420), a second insulation layer (425) and a hard mask (430) are formed on the lower insulation layer (400) formed with a copper lower

interconnection (405), and an interconnection trench, a winding-shaped first trench and a via hole are formed. Subsequently, a first barrier metal (445) is deposited, and a copper interconnection (452) in the interconnection trench, a first copper interconnection in the first trench and a via contact plug are formed. Subsequently, a photoresist pattern is formed to expose the region to be formed with a capacitor later, a winding-shaped second trench (454) is formed by using the photoresist pattern and removing the exposed second insulation layer.

The subsequent processes are different from the first embodiment. A winding-shaped third trench (456) is formed in the first barrier metal by removing the first copper interconnection of the capacitor region (A).

Fig. 4 is a cross-sectional view showing a second insulation layer (425) of the capacitor region (A) where a first copper interconnection is removed. In the region where the second insulation layer is removed, a second trench (454) is formed and in the region where the first copper interconnection is removed, a third trench (456) is formed.

Since the first copper interconnection needs to be etched in the capacitor region (A) only, a photo process is performed so that the copper interconnection in the metal interconnection region (B) should not be damaged. A three-dimensional structure of the first barrier metal (445) is formed by removing the second insulation layer and the first copper interconnection, as shown in Fig. 4. Then, HCl or H_2SO_4

acid solution is used to etch the first copper interconnection only without damaging the first barrier metal.

After the formation of a three-dimensional structure of the first barrier metal (445) only, the process same as the processing order of the first embodiment in Figs. 2f and 2g is performed. That is, a first electrode, a dielectric layer and a second electrode are formed to form a capacitor. Subsequently, a second barrier metal is deposited, and after the deposition of a second copper conductive layer, a capacitor is formed in the same layer as the copper interconnection by performing the CMP.

Therefore, the second embodiment is proceeded in the same processing as those in Figs. 2a to 2e of the first embodiment, and a process of Fig. 4 that removes the first copper conductive layer in HCl or H_2SO_4 acid solution is added.

In the second embodiment, a first barrier metal is formed in a winding shape, and the second copper interconnection and the capacitor are formed at what is supposed to be a part for an insulation layer and a part for the first copper interconnection conventionally. That is, with the first barrier metal in the center, a capacitor composed of a first electrode on both sides and at the bottom, a dielectric layer, a second electrode, a second barrier metal and a second copper interconnection is formed.

In other words, the semiconductor including the capacitor comprises: a barrier metal with a winding-shaped first trench (the winding-shaped third trench) inside; a second trench (a

winding-shaped second trench) formed between the barrier metal; and a capacitor formed with a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the first and the second trenches.

Compared to the first embodiment, the second embodiment has an advantage that the capacitor area increases further.

The above embodiment describes about a copper damascene, but the same interconnection process can be performed in the other conductive metal, oxide metal or conductive compounds other than copper, and the same capacitor can be formed.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.

[Effect of Invention]

The present invention described above forms a capacitor without increasing the number of processing steps by fabricating a capacitor in the same layer as the metal interconnection, maintaining the damascene process for forming a conventional interconnection.

Also, the structure of the capacitor can be embodied easily by the damascene process, thus obtaining a capacitance of high capacity which is needed for logic elements.

[Claims]

1. A method for forming a semiconductor device, comprising the steps of:

forming an insulation layer in a capacitor region and a metal interconnection region on a substrate;

forming a metal interconnection at the metal interconnection region of the insulation layer by performing a dual damascene process; and

forming a capacitor in the same layer as the metal interconnection in the insulation layer of the capacitor region.

2. The method as recited in claim 1, wherein the forming a capacitor includes the steps of:

forming a first trench at the capacitor region of the insulation layer;

forming a first metal interconnection inside the first trench;

forming a second trench by removing the insulation layer between the first metal interconnection; and

forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench.

3. The method as recited in claim 1, wherein the forming a capacitor includes the steps of:

forming a first trench in the capacitor region of the insulation layer;

forming a first barrier metal and a first metal interconnection inside the first trench;

forming a second trench by removing the insulation layer around the first barrier metal;

forming a third trench in the first barrier metal by removing the first metal interconnection; and

forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches.

4. The method as recited in claim 2 or 3, further comprising the step of forming a second metal interconnection connected to the second electrode of the capacitor.

5. The method as recited in claim 2 or 3, wherein the first metal interconnection is of copper.

6. The method as recited in claim 2 or 3, wherein the first and the second electrodes are of a metal selected from a group of Pt, Ru, Ir and W.

7. The method as recited in claim 2 or 3, wherein the dielectric layer is of an oxide selected from a group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.

8. A method for fabricating a semiconductor device, comprising the steps of:

forming an insulation layer including a first and a second insulation layers in the capacitor region and the metal interconnection region on a substrate formed with a lower conductive layer;

forming an interconnection trench in the metal insulation region, a first trench in the capacitor region and a via hole connected to the lower conductive layer by selectively etching the insulation layer;

forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them;

forming a second trench by selectively forming the second insulation layer of the capacitor region;

forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second trench; and

forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

9. A method for fabricating a semiconductor device, comprising the steps of:

a) forming an insulation layer including a first and a second insulation layers in the metal interconnection region

and the capacitor region on the substrate formed with a lower conductive layer;

b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer;

c) forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first copper layer in the interconnection trench, the via hole and the first trench and planarizing them;

d) forming a second trench by selectively etching the second insulation layer around the first copper interconnection in the capacitor region;

e) forming a third trench in the first barrier metal by selectively etching the first copper interconnection;

f) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the second and the third trenches; and

g) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing it.

10. The method as recited in claim 8 or 9, wherein the insulation layer includes an etching blocking layer between the first insulation layer and the second insulation layer.

11. The method as recited in claim 8 or 9, further including a hard mask on the second insulation layer.

12. The method as recited in claim 8 or 9, wherein the forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer forms the interconnection trench and the first trench simultaneously first, and then forming the via hole.

13. The method as recited in claim 8 or 9, wherein the forming an interconnection trench, a via hole and a first trench by selectively etching the insulation layer forms the via hole first, and then forming the interconnection trench and the first trench simultaneously.

14. The method as recited in claim 8 or 9, wherein the first and the second copper conductive layers use a reflow method after forming a layer in a sputtering method, a CVD method or an electroplating method.

15. The method as recited in claim 14, wherein in case of using the electroplating method, a seed layer is formed in a method selected from a group of a physical vapor deposition (PVD), a chemical vapor deposition (CVD) and an electroless deposition, or a combination thereof.

16. The method as recited in claim 8, further including the steps of:

g) forming a first barrier metal prior to the first copper layer; and

h) forming a second barrier metal prior to the second copper layer.

17. The method as recited in claim 9, wherein a second barrier metal is formed prior to the formation of the second copper layer.

18. The method as recited in claim 9, 16 or 17, wherein the first and the second barrier metals is of one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN, and a combination thereof.

19. A semiconductor device, comprising:

a substrate;

an insulation layer formed in the metal interconnection region and the capacitor region on the substrate;

a metal interconnection in the insulation layer of the metal interconnection; and

a capacitor formed in the same layer as the metal interconnection in the capacitor region of the insulation layer.

20. The semiconductor device as recited in claim 19, wherein the capacitor includes:

a first metal interconnection;

a trench formed between the first metal interconnection; and

a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the trench.

21. The semiconductor device as recited in claim 17, wherein the capacitor includes:

a barrier metal with a first trench inside;

a second trench formed between the barrier metal; and

a capacitor composed of a first electrode, a dielectric layer and a second electrode on the side and the bottom surfaces of the first and the second trench.

22. The semiconductor device as recited in claim 20 or 21, further including a second metal interconnection connected to the second electrode of the capacitor.

23. The semiconductor device as recited in claim 20 or 22, wherein the first and the second metal interconnections are formed by depositing the copper layer and the barrier metal.

24. The semiconductor device as recited in claim 19, wherein the insulation layer is of a material selected from a group of SiO_2, SiOC, SiOH, SiOCH, insulation layers with dielectric constants below 3.0, and a combination thereof.

25. The semiconductor device as recited in claim 20 or 21, wherein the dielectric layer is of an oxide selected from a

group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.

26. The semiconductor device as recited in claim 20, wherein the first and the second electrodes are of a metal selected from a group of Pt, Ru, Ir and W.

27. The semiconductor device as recited in claim 23, wherein the barrier metal is of a material selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN, TaSiN, and a combination thereof.